SPECIFICATION AMENDMENTS

Please amend the specification as follows:

Amend the paragraph starting on page 13, line 25, through page 14, line1 as follows:

-- The signal is VREF is inputted into a base of the third transistor Q3, and the signal PDIN is inputted into a base of the fourth transistor Q4. Referring to FIGS. 2 and 4, the base of the third transistor Q3 corresponds to ~~an inverter~~ a non-inverting terminal of the differential amplifier G1 to receive the reference potential VREF, and the base of the fourth transistor Q4 corresponds to ~~a non-inverter~~ an inverting terminal of the differential amplifier G1. --

Page 20, amend the paragraph starting on line 6 as follows:

-- FIG. 11 is a circuit diagram showing another current detecting limiter unit 11-4 of the current-voltage transforming circuit ~~shown in FIG. 10~~. The current detecting limiter unit 11-4 can be used in the current-voltage transforming circuit shown in FIGS. 2 and 5. --

Page 21, amend the paragraph starting on line 7 as follows:

-- FIG. 12 is a circuit diagram showing another current detecting limiter unit 11-5 ~~using a PNP type transistor having a high amplification constant ß in~~ of the current-voltage transforming circuit ~~shown in FIG. 10~~. The current detecting limiter unit 11-5 can be used in the current-voltage transforming circuit shown in FIGS. 2 and 5. --